a second conductivity type semiconductor layer formed at a first area of the well area which is isolated by the element isolation areas, the semiconductor layer configuring a first electrode of a capacitor; and

a first conductivity type low resistance area provided at a base portion of the well area, the low resistance area having a resistive value lower than that of the well area,

wherein the low resistance area is not in contact with a depletion layer of a junction portion between the semiconductor layer and the well area and is in contact with the element isolation areas.

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7. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

an MOS transistor formed in a first area of the well which is isolated by the element isolation areas; and

a first conductivity type low resistance area provided at a base portion of the well area an having a resistive value lower than that of the well area,

wherein the low resistance area is not in contact with a depletion layer of a junction portion between source/drain regions of the MOS transistor and is in contact with the element isolation areas.

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13. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first conductivity type well area formed in a surface area of the semiconductor substrate;

a plurality of element isolation areas formed in the well area;

a second conductivity type base layer formed on the well area which is isolated by the element isolation areas, the well area configuring a first electrode of a bipolar transistor;

a first conductivity type second electrode formed on the base layer; and

a first conductivity type low resistance area provided at the base portion of the well area, the low resistance area having a resistive value lower than that of the well area,

wherein the low resistance area is not in contact with a depletion layer of a junction portion of the bipolar transistor and is in contact with the element isolation areas.

16. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a first well area formed in a surface area of the semiconductor substrate;

a second well area formed in a surface area of the semiconductor substrate;

an analog circuit formed in the first well area;

a digital circuit formed in the second well area;

an isolation area formed between the first and second well area; and

a first conductivity type low resistance area provided at a base portion of the first well area, the first conductivity type low resistance area having a resistive value lower than that of the first well area,

wherein the low resistance area is not in contact with a depletion layer of the analog circuit and in contact with the isolation area.